UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/982,020	10/19/2001	Peter Markstein	10008023-1	7131

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EXAMINER
PHAM, CHRYSTINE

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/982,020	MARKSTEIN ET AL.
	Examiner	Art Unit
	Chrystine Pham	2122

-- *The MAILING DATE f this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *19 October 2001*.

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-31* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-31* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *19 October 2004* is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   This action is responsive to application 09/982020 filed on October 19th 2001.

2.   Claims 1-31 are presented for examination.

Claim Rejections - 35 USC § 102

3.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for

the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4.   Claims 1, 2, 4-16, 18-21, 23-28, 30, 31 are rejected under 35 U.S.C. 102(b) as being anticipated

by Aizikowitz et al. (US 5890000), hereinafter, *Aizikowitz et al.*.

Claim 1

Aizikowitz et al. teach a method of allocating registers (e.g., see *Register allocation* col.1:24-67) when

compiling source code (e.g., see *source code, intermediate language instructions* col.4:9-20 & associated

text; see *12* Fig.1 & associated text), said method comprising steps of:

   o   translating source code to intermediate code (e.g., see *source code, intermediate*

        language instructions col.4:9-20 & associated text; see *12* Fig.1 & associated text);

   o   identifying an operand from said intermediate code (e.g., see *data items* col.1:24-35 &

        associated text; see *data item, variable "c"* col.2:15-35 & associated text) to store in a

        real register (e.g., see *"Register allocation", physical hardware* col.1:24-35; *local register*

        allocator, hardware registers col.1:49-57 & associated text; see *14* Fig.1 & associated

        text); and

   o   selecting a class of real registers operable to store said operand (e.g., see *local register*

        allocator, global register allocator col.1:49-67 & associated text).

Claim 2

The rejection of base claim 1 is incorporated. *Aizikowitz et al.* further teach selecting at least one subclass of said selected class of real registers, wherein said at least one subclass includes a register to store said operand (e.g., see *local register allocator, global register allocator* col.1:49-67 & associated text; col.4:40-46; see *18, 20, 22* Fig.2 & associated text).

Claim 4

The rejection of base claim 2 is incorporated. *Aizikowitz et al.* further teach wherein said step of selecting at least one subclass further comprises steps of:

- o selecting a first set of subclasses within said selected class (e.g., see *register allocation* col.1:24-67 & associated text; see *live range* col.2:15-35 & associated text; see *assigning live ranges* col.2:35-55 & associated text);

- o determining whether a register included in said first set of subclasses is available to store said operand (e.g., see *local, global* col.1:35-67 & associated text; see *assigning live ranges* col.2:35-55 & associated text; see *register pressure, spilling* col.2:35-65 & associated text; see *16-22* Fig.2 & associated text); and

- o in response to said register being available, storing said operand in said register (e.g., col.2:35-65; see *16-22* Fig.2 & associated text).

Claim 5

The rejection of base claim 4 is incorporated. *Aizikowitz et al.* further teach wherein said first set of subclasses includes at least one of non-used-in-current-operation, non-busy, non-live and non-used subclasses (e.g., see *defined and then used within only a single basic block* col.1:35-48; see *lifetime* col.1:49-57; see *26, 28* Fig.3 & associated text).

Claim 6

The rejection of base claim 4 is incorporated. *Aizikowitz et al.* further teach wherein said step of

selecting at least one subclass further comprises steps of:

- o selecting a second (or third or fourth) set of subclasses within said selected class in response to

  said register not being available in said first (or second or third) set of subclasses (e.g., see *first*

  register allocator, second register allocator, remaining portions col.3:25-50; see *16-22* Fig.2 &

  associated text);

- o determining whether a register included in said second (or third or fourth) set of subclasses is

  available to store said operand (e.g., see *local allocator, global allocator* col.3:25-51; see *local,*

  global col.1:35-67 & associated text; see *assigning live ranges* col.2:35-55 & associated text;

  see *register pressure, spilling* col.2:35-65 & associated text; see *16-22* Fig.2 & associated text);

  and

- o in response to said register in said second (or third or fourth) set of subclasses being available,

  storing said operand in said register in said second (or third or fourth) set of subclasses (e.g.,

  col.2:35-65; see *16-22* Fig.2 & associated text).

Claim 7

The rejection of base claim 6 is incorporated. *Aizikowitz et al.* further teach wherein said second set of

subclasses includes at least one of non-used-in-current-operation, non-busy, non-live (see claim 5) and

used subclasses (e.g., see *global, use of register* col.1:40-48 & associated text; see *lifetime overlaps,*

uses col.1:49-57 & associated text).

Claim 8

The rejection of base claim 6 is incorporated. Claim recites limitations, which have been addressed in

claim 6, therefore, is rejected for the same reasons as cited in claim 6.

Claim 9

The rejection of base claim 8 is incorporated. *Aizikowitz et al.* further teach wherein said third set of subclasses includes at least one of non-used-in-current-operation, live, and non-busy subclasses (e.g., see *global lifetimes, lifetime overlaps* col.1:49-57 & associated text; see *live ranges* col.3:25-50 & associated text; see *26, 30* Fig.3 & associated text).

Claim 10

The rejection of base claim 8 is incorporated. Claim recites limitations, which have been addressed in claim 6, therefore, is rejected for the same reasons as cited in claim 6.

Claim 11

The rejection of base claim 10 is incorporated. *Aizikowitz et al.* further teach wherein said fourth set of subclasses includes at least one of non-used in current operation and busy subclasses (e.g., see *same register* col.2:35-40 & associated text).

Claim 12

The rejection of base claim 11 is incorporated. *Aizikowitz et al.* further teach spilling a register in at least one of said busy and said live subclasses prior to storing said operand in said register in at least one of said busy and said live subclasses (e.g., see *register pressure, spilling* col.2:35-65 & associated text).

Claim 13

The rejection of base claim 11 is incorporated. *Aizikowitz et al.* further teach storing said operand in a class (i.e., selected other class) other than <u>selected class</u> in response to a register in said fourth set of subclasses not being available (i.e., <u>selected class</u> of registers not including a not-used-in-current-operation register) (e.g., see *local allocator, global allocator* col.3:25-51; see *local, global* col.1:35-67 & associated text; see *assigning live ranges, K registers* col.2:35-65 & associated text; see *different hardware register* col.4:32-52; see *16-22* Fig.2 & associated text).

Claim 14

The rejection of base claim 11 is incorporated. *Aizikowitz et al.* further teach marking said register as used-in-current-operation in response to storing said operand in said register (e.g., col.2:35-40).

Claim 15

The rejection of base claim 11 is incorporated. *Aizikowitz et al.* further teach marking said register storing said operand as live and not-used-in-current-operation in response to translating an instruction of said source code (e.g., see *26, 30* Fig.3 & associated text).

Claim 16

The rejection of base claim 1 is incorporated. Claim recites limitations, which have been addressed in claim 13, therefore, is rejected for the same reasons as cited in claim 13.

Claim 18

A method of (i.e., a compiler configured to) compiling source code comprising steps of:

o generating intermediate code from a portion of source code (e.g., ., see *source code, intermediate language instructions* col.4:9-20 & associated text; see *12* Fig.1 & associated text);

o allocating a plurality of real registers to store a plurality of operands from said intermediate code while generating the intermediate code (i.e., register allocation stage) (e.g., see *"Register allocation", physical hardware* col.1:24-35; *local register allocator, hardware registers* col.1:49-57 & associated text; see *14* Fig.1 & associated text); and

o optimizing stage configured to optimize said intermediate code (e.g., see *optimizing compilers* col.4:9-21)

o a final code stage generating machine-readable code from said intermediate code using said plurality of real registers (e.g., see *machine-readable object code* col.4:9-21).

Claim 19

The rejection of base claim 18 is incorporated. *Aizikowitz et al.* further teach a plurality of types of

operands and said step of allocating further comprises steps of:

- o   determining a type of operand for at least one of said plurality of operands (e.g., see *local register*

     allocator, global register allocator col.1:49-67 & associated text);

- o   storing said at least one operand in memory (i.e., selected class of real registers) in response to

     said operand being a particular type of operand (i.e., selecting a class of registers depending on

     said type of operand) (e.g., see *symbolic register, local, global* col.1:35-67 & associated text; see

     24 Fig.3 & associated text; see *RAM* col.5:53-65); and

- o   allocating a real register (from said selected class of registers depending on said type of said

     operand) for said operand (e.g., see *"Register allocation", physical hardware* col.1:24-35; see

     local register allocator, global register allocator col.1:49-67 & associated text; see *28, 30, 32, 34*

     Fig.3 & associated text).

Claim 20

The rejection of base claim 19 is incorporated. *Aizikowitz et al.* further teach wherein said particular type

of operand includes a local variable (e.g., see *symbolic register, local, global* col.1:35-67 & associated

text; see *variable "c"* col.2:15-35 & associated text).

Claim 21

The rejection of base claim 19 is incorporated. Claim recites limitations, which have been addressed in

claim 19, therefore, is rejected for the same reasons as cited in claim 19.

Claim 23

The rejection of base claim 21 is incorporated. Claim recites limitations, which have been addressed in

claim 2, therefore, is rejected for the same reasons as cited in claim 2.

Claim 24

The rejection of base claim 23 is incorporated. Claim recites limitations, which have been addressed in claims 5, 7, 9, 11, therefore, is rejected for the same reasons as cited in claims 5, 7, 9, 11.

Claim 25

Claim recites a compiler version performing the method addressed in claim 18, therefore, is rejected for the same reasons as cited in claim 18.

Claim 26

The rejection of base claim 25 is incorporated. Claim recites limitations, which have been addressed in claim 19, therefore, is rejected for the same reasons as cited in claim 19.

Claim 27

The rejection of base claim 26 is incorporated. Claim recites limitations, which have been addressed in claim 20, therefore, is rejected for the same reasons as cited in claim 20.

Claim 28

The rejection of base claim 25 is incorporated. Claim recites limitations, which have been addressed in claim 19, therefore, is rejected for the same reasons as cited in claim 19.

Claim 30

The rejection of base claim 28 is incorporated. Claim recites limitations, which have been addressed in claim 2, therefore, is rejected for the same reasons as cited in claim 2.

Claim 31

The rejection of base claim 30 is incorporated. Claim recites limitations, which have been addressed in claims 5, 7, 9, 11, therefore, is rejected for the same reasons as cited in claims 5, 7, 9, 11.

Claim Rejections - 35 USC § 103

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness

rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
section 102 of this title, if the differences between the subject matter sought to be patented and the prior art
are such that the subject matter as a whole would have been obvious at the time the invention was made to
a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be
negatived by the manner in which the invention was made.

6.   Claims 3, 17, 22, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Aizikowitz et*

al. in view of Lueh et al. (US 6292935), hereinafter, *Lueh et al..*

Claim 3

The rejection of base claim 1 is incorporated. *Aizikowitz et al.* further teach wherein said selected class

includes one of a callee-saved class (i.e., in response to said operand including at least one of local

variables, stack items and parameters input by a user). *Aizikowitz et al.* do not expressly disclose a

caller-saved class (i.e., in response to said operand including a temporary computation). However, *Lueh*

et al. disclose a caller-saved class (i.e., in response to said operand including a temporary computation)

(e.g., see *caller-saved Register* col.6:62-col.7:2). *Aizikowitz et al.* and *Lueh et al.* are analogous art

because they are both directed to optimizing compilers and physical (i.e., real) register allocation. It

would have been obvious to one of ordinary skill in the pertinent art at the time the invention was made

to incorporate the teaching of *Lueh et al.* into that of *Aizikowitz et al.* for the inclusion of a caller-saved

class. And the motivation for doing so would have been to facilitate the categorization of registers based

on the types of operands stored therein so that optimization can be performed by taking actions

corresponding to different categories of registers as taught by *Lueh et al.* (i.e., generating spills only for

operands stored in caller-saved registers) (e.g., col.6:62-col.7:2)..

Claim 17

The rejection of base claim 3 is incorporated. Claim recites limitations, which have been addressed in

claim 3, therefore, is rejected for the same reasons as cited in claim 3.

Claim 22

The rejection of base claim 21 is incorporated. Claim recites limitations, which have been addressed in claim 3, therefore, is rejected for the same reasons as cited in claim 3.

Claim 29

The rejection of base claim 28 is incorporated. Claim recites limitations, which have been addressed in claim 3, therefore, is rejected for the same reasons as cited in claim 3.

Conclusion

7.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Grove et al. (US 5659754)

Sato (US 5261062)

Radigan (US 6738967)

Goebel (US 5901317)

Goebel (US 5418958)

Gschwind et al. (US 6513109)

Munshi et al. (US 4782444)

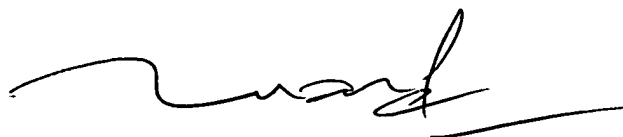Koblenz et al. (US 5530866)

8.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chrystine Pham whose telephone number is 571.212.3702. The examiner can normally be reached on Mon-Fri, 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q Dam can be reached on 571.272.3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application

Information Retrieval (PAIR) system. Status information for published applications may be obtained from

either Private PAIR or Public PAIR. Status information for unpublished applications is available through

Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC)

at 866-217-9197 (toll-free).

December 3, 2004

TUAN DAM
SUPERVISORY PATENT EXAMINER